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A fully integrated analog front end circuit, wireless transceiver, and DSP for ECG monitoring SOC

應用於 ECG 生醫信號監測的類比前端與無線收發系統整合晶片

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作品摘要

隨著高齡化社會的來臨，遠距醫療照護漸漸成為了現在進行式，其中心電信號的即時監測更是預防國人因慢性疾病而導致不可挽回之意外的重要課題。目前常見的產品中主要利用數個單晶片的組合來達到此功能，這導致產品體積過於龐大，而過大的功率消耗必須時常替換電池更增加使用的麻煩。故我們提出一低功率心電訊號（ECG）監測無線傳輸系統整合晶片，包括前端的低雜訊低功率放大器（Low noise/power Amplifier）、漸進比較式（SAR）類比數位轉換器、無線收發機（Wireless Transceiver）、以及數位處理電路單元（ECG特徵擷取電路）。本系統晶片更針對IEEE既有文獻中晶片主要功率消耗的部分進行改良，創新提出低功率高資料傳輸量之無線收發機。

由於早期MICS band的通道頻寬只有100 kHz或300 kHz，資訊傳輸量過低，對於生醫應用稍嫌不足，因此FCC另外制定出Med-radio band的頻帶提供較寬的通道以符合實際傳輸需求。為了達到Med-radio band低功率的要求，我們在發射機使用相位選擇器（Phase MUX）以及邊緣結合器（Edge Combiner）來實現高頻譜效率的D-BPSK調變；而接收機則使用無須參考頻率的動態相位對振幅轉換技巧來實現D-BPSK解調。以相位選擇器作載波調變比起以往傳統電路架構來的簡單且不易受環境變異以及元件匹配因素所影響，加上邊緣合成器可降低頻率產生電路的操作頻率，有利於實現低功率消耗以及高傳輸效率。接收機方面由於不需要大量消耗功率的鎖相迴路提供精準的相位做D-BPSK解調，可達成低功率消耗的目標。

本系統晶片的創新及完整度部分整理如下:

1. 提出創新的低功率無線收發器，以D-BPSK的調變模式在短距離傳輸（1~2m）達到10Mbps的高資料傳輸量
2. 提出一數位處理單元電路，包含ECG訊號特徵擷取（Feature Extraction）模式
3. 結合類比前端低雜訊放大器（<2μW），類比數位轉換器（<10μW），數位處理單元電路（<300μW），低功率高資料量的無線收發機（<2.1mW），整體系統晶片消耗約2.4mW，為極低的功率消耗

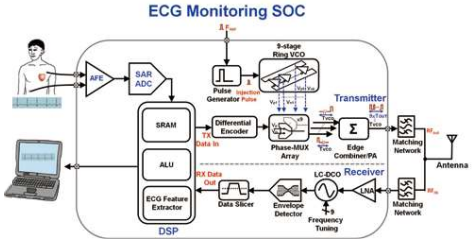

圖1 > 晶片之系統架構圖

2014

指導教授

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於 2001 取得美國加州大學洛杉磯校區（UCLA）博士學位，曾任職於博通（Broadcom Corporation）參與類比 / 射頻 / 混合訊號電路設計，並開發無線傳輸系統。2004 年加入臺灣大學電子工程學研究所擔任助理教授，2011 年升任教授。

研究領域

生醫應用高能量效率無線通訊晶片，應用於 PLL 與 Delta-Sigma ADC 之混合信號電路設計技術，以及感測器與生醫應用類比訊號處理電路。

指導教授

馬席彬 / 清華大學電機工程學系

分別於 1995 年跟 2002 年取得臺灣大學學士以及博士學位，並於 2003 年進入清華大學電機工程學系任教，現任職於清華大學電機工程學系與研究所副教授。

研究領域

通訊系統設計及 SoC 實作、生醫訊號處理及應用實作、智慧型手機感測器及整合應用。

Abstract

As the population is ageing in our society, the tendency is developing convenient and safe medical electric equipment. With the development of semiconductor technology, biomedical electronic systems execute signal amplification and processing with integrating several chips instead of bulky apparatus composed of transistor modules and discrete circuit elements. The evolution of very-large-scale integration technology not only results in portable medical equipment widespread gradually but reveals medical telehealth caring era: patients stay home and the bioelectronic equipment monitors their physical conditions, then the amplified sensing-signals transfer to remote hospital via wireless transmission system on time and immediately. The doctors in the hospital can discover any abnormal physical situation and take emergency treatment.

However, medical products have to replace batteries frequently for high power consumption, and the discrete electric elements of the products, such as amplifiers, AD converters, and wireless transmitter, are bulky as well as expensive. The outstanding research teams focus on developing SOC which integrates all circuits in a chip, and emphasize on improving low power consumption, low noise, high resolution, and efficiency.

This system-on chip integrates ECG real time monitoring system with wireless transceiver, including low noise/power amplifier, SAR AD converter, wireless transceiver, ECG feature extraction circuitry. Most of literatures published on IEEE symposium and journals pointed out large power consumption generally. The main power consumption is wireless transceiver and DSP. This SOC will solve problems as mentioned above, and not only integrate front-end circuit and DSP but reveal an innovative wireless transceiver architecture for low power consumption and high data rate.

Recently, FCC allocated a new and wider radio band called MedRadio band to replace the early MICS which only has less than 100k data rate. For low power requirement in MedRadio band, phase MUX and edge combiner technique are utilized in the transmitter to implement high bandwidth efficiency modulation scheme, D-BPSK. In the receiver, a reference-less dynamic phase to amplitude scheme is adopted to demodulate D-BPSK signal from the transmitter. The transmitter is much immunity to noise from environment and PVT (process, supply voltage, and temperature) in CMOS process. Furthermore, carrier frequency is generated by edge-combiner based PA and multi-phase low frequency oscillator, which significantly reduces power of the transmitter. By phase-MUX technique, the transmitter can support high data rate. A power-hungry PLL is not necessary in the demodulation phase, which achieves low power purpose in the receiver.

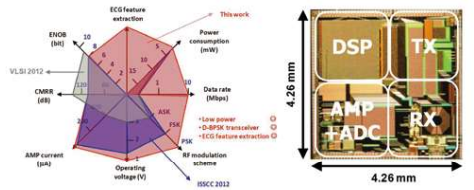

Fig.2 > The SoC benchmark and chip microphotograph

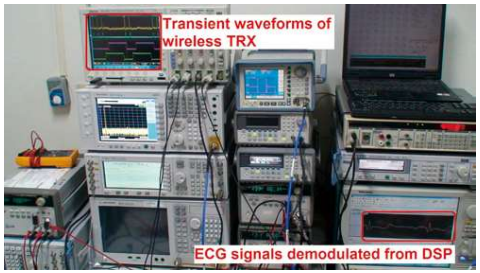

Fig.3 > The demonstration of the bio-signal monitoring SoC